Amendments to the Claims:

1. (original) A phase-locked loop, comprising:

a phase-frequency detector coupled to receive a reference signal, wherein the phase-frequency detector produces a phase control signal based upon a difference in phase between the reference signal and a low noise divided signal;

a charge pump for producing a voltage controlled oscillator (VCO) control signal based upon the phase control signal;

a VCO for producing an oscillation having a frequency based upon the VCO control signal; and

a low-noise divider for producing the low phase noise divided oscillation, wherein the low-noise divider further includes:

a pulse-swallow configured divider module for producing a pre-scaled divider output based upon the oscillation produced by the VCO and a divided oscillation based upon the pre-scaled divider output;

a first latching block for latching the divided oscillation based upon the pre-scaled divider output as a clock to produce a first latched signal;

a second latching block for latching the first latched signal based upon the VCO oscillation as a clock to produce a second latched signal; and

a third latching block for latching the second latched signal based upon the VCO oscillation as a clock to produce a third latched signal, which third latched signal is the low phase noise divided oscillation and is produced to the phase-frequency detector for comparison to the reference signal.

2. (original) The phase-locked loop of claim 1 wherein the first and second latching blocks are biased by a first bias signal and wherein the third latching block is biased by a second bias signal.

3. (original) The phase-locked loop of claim 2 wherein the second bias signal is greater in magnitude than the first bias signal.

4. (original) The phase-locked loop of claim 3 wherein the first, second and third latching blocks each contain an output load device and wherein the output load device of the third latching block has a smaller impedance than an impedance of the output load devices of the first and second latching blocks.

5. (original) The phase-locked loop of claim 1 wherein the pulse-swallow configured divider further includes a pre-scaled divider block and first and second divider blocks wherein the pre-scaled divider block is biased by a first bias signal and wherein the first and second divider blocks are biased for digital operation.

6. (original) The phase-locked loop of claim 5 wherein the first and second latching blocks are biased by the first bias signal and wherein the third latching block is biased by a second bias signal.

7. (original) The phase-locked loop of claim 6 wherein the second bias signal is greater than the first bias signal.

8. (original) The phase-locked loop of claim 1 further including a buffer coupled between the VCO and the low-noise divider wherein the buffer produces a buffered oscillation and wherein the pulse-swallow configured divider module produces the pre-scaled divider output based upon the buffered oscillation produced by the buffer.

9. (original) The phase-locked loop of claim 8 wherein the third latching block is clocked by the VCO oscillation and the second latching block is clocked by the buffered oscillation.

10. (original) A divider for producing a low phase noise divided oscillation, comprising:

a pulse-swallow configured divider module for producing a pre-scaled divider output based upon an oscillation produced by a frequency source and a divided oscillation based upon the pre-scaled divider output;

a first latching block for latching the divided oscillation based upon the pre-scaled divider output as a clock to produce a first latched signal;

a second latching block for latching the first latched signal based upon the frequency source oscillation as a clock to produce a second latched signal; and

a third latching block for latching the second latched signal based upon the frequency source oscillation as a clock to produce a third latched signal, which third latched signal is the low phase noise divided oscillation.

11. (original) The divider of claim 10 wherein the first and second latching blocks are biased by a first bias signal and wherein the third latching block is biased by a second bias signal, which second bias signal is greater in magnitude than the first bias signal.

12. (original) The divider of claim 11 wherein the first latching block is clocked by the pre-scaled divider output and wherein the third latching block is clocked by the low phase noise oscillation.

13. (original) The divider of claim 12 wherein the first, second and third latching blocks each contain an output load device wherein the output load device of the third latching block has a smaller impedance value than the impedance value of the first and second latching block output load devices.

14. (currently amended) The divider of claim 10 wherein the pulse-swallow configured divider module further includes a pre-scaled divider block and first and second divider blocks wherein the pre-scaled divider block is biased by the first bias signal ~~and wherein the first and second divider blocks are biased for digital operation~~.

15. (original) The divider of claim 14 wherein the second bias signal is greater than the first bias signal.

16. (original) The divider of claim 10 further including a buffer coupled between the frequency source and the divider wherein the buffer produces a buffered oscillation wherein the pulse-swallow configured divider module produces the pre-scaled divider output based upon the buffered oscillation produced by the frequency source.

17. (original) The divider of claim 16 wherein the third latching block is clocked by the frequency source oscillation and the second latching block is clocked by the buffered oscillation.

18. (original) A method for producing a low phase noise divided oscillation, comprising:

producing a pre-scaled divider output based upon an oscillation produced by a frequency source;

producing a divided oscillation based upon the pre-scaled divider output;

latching the divided oscillation based upon the pre-scaled divider output as a clock to produce a first latched signal;

latching the first latched signal based upon the frequency source oscillation as a clock to produce a second latched signal; and

latching the second latched signal based upon the frequency source oscillation as a clock to produce a third latched signal, which third latched signal is the low phase noise divided oscillation.

19. (original) The method of claim 18 wherein first and second latching blocks are biased by a first bias signal and wherein a third latching block is biased by a second bias signal.

20. (original) The method of claim 19 wherein the second bias signal is greater in magnitude than the first bias signal.

21. (original) The method of claim 20 wherein the first, second and third latching blocks each contain an output load device and wherein the output load device of the third latching block has a smaller impedance value than the impedance value of the output load devices of the first and second latching blocks.

22. (currently amended) The method of claim 18 wherein a pulse-swallow configured divider module further includes a pre-scaled divider block and first and second divider blocks wherein the pre-scaled divider block is biased by a first bias ~~signal and wherein the first and second divider blocks are biased for digital operation~~.

23. (original) The method of claim 22 wherein the second bias signal is greater than the first bias signal.

24. (original) The method of claim 18 further including a buffer coupled between the frequency source and a divider wherein the buffer produces a buffered oscillation wherein a pulse-swallow configured divider module produces the pre-scaled divider output based upon the buffered oscillation produced by the buffer.

25. (original) The method of claim 24 wherein a first latching block is clocked by the pre-scaled divider output and a second latching block is clocked by the buffered oscillation and a third latching block is clocked by the frequency source oscillation.

26. (currently amended) A method for producing a low-noise divided oscillation, comprising:

latching a divided signal based upon a pre-scaled divider output to produce a first latched signal wherein the pre-scaled divider output is based upon an oscillation;

latching the first latched signal based upon the oscillation to produce a second latched signal;

latching the second latched signal based upon the oscillation to produce the low-noise divided oscillation;

biasing first and second latching blocks that perform the steps of latching the divided signal and latching the first latched signal at a first bias level; and

biasing a third latching block that performs the step of latching the second latched signal at a second bias level.

27. (original) The method of claim 26 further including buffering the oscillation to produce a buffered oscillation wherein the pre-scaled divider output is based upon the buffered oscillation and further wherein the step of latching the first latched signal is based upon the buffered oscillation.

28. Cancelled.

29. Cancelled.

30. (currently amended) A divider for producing a low phase noise divided oscillation, comprising:

a multi-modulus divider module for producing a divided oscillation based upon an oscillation produced by a frequency source and a modulus control signal;

a first latching block for latching the divided oscillation based upon the frequency source oscillation as a clock to produce a first latched signal; [[and]]

a second latching block for latching the first latched signal based upon the frequency source oscillation as a clock to produce a second latched signal, which second latched signal is the low phase noise divided oscillation;

wherein the first and second latching blocks are biased by a first bias signal and further including a third latching block wherein the third latching block is biased by a second bias signal, which second bias signal is greater in magnitude than the first bias signal; and

wherein the first and second latching blocks each contain an output load device wherein the output load device of the second latching block has a smaller impedance value than the impedance value of the first latching block output load device.

31. Cancelled.

32. Cancelled.

33. (original) The divider of claim 30 wherein the multi-modulus divider module further includes a plurality of divider blocks operably coupled to produce the divided oscillation based on the modulus control signal and the frequency source oscillation divided by at least one of a first divisor and a second divisor.

34. (original) The divider of claim 30 further including a buffer coupled between the frequency source and the multi-modulus divider module wherein the buffer produces a buffered oscillation wherein the multi-modulus divider module produces the divided oscillation output based upon the buffered oscillation produced by buffer.

35. (currently amended) The divider of claim 34 wherein the second latching block is clocked by the ~~frequency source oscillation and the first latching block is clocked by the~~ buffered oscillation.